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(71) Applicant: Hughes Aircraft Company
7200 Hughes Terrace P.O.Box 45066
Los Angeles California 90045-0066(US)

(72) Inventor: Berman, Arnold L.
714 Claymont Drive
Los Angeles California 90049(US)
Inventor: Hahn, Carl J., III
430 West 64th Street
Inglewood California 90302(US)
Inventor: Wachs, Marvin R.
22555 Paul Revere Drive
Woodland Hills California 91364(US)

(74) Representative: Witte, Alexander, Dr.-Ing.
Augustenstrasse 7
D-7000 Stuttgart 1(DE)

(54) **Self equalizing multi-stage radio frequency power amplifier.**

(57) Linearity and efficiency of a radio frequency two-stage power amplification device (10) are increased by employing two tuned circuits 16 and 18 in a driver stage (12) and two tuned circuits (22 and 24) in a high power stage (14). After selecting elements of tuned circuits (22 and 24) in order to optimize the high power stage (14) for efficiency, linearity and power output, elements are selected for tuned circuits (16 and 18) in order to cause the intermodulation output components associated with the driver stage (12) to have a 180° phase angle relative to the intermodulation output components associated with the individual high power stage (14). This phase angle relationship will cause the intermodulation output component products from the driver and high power stages (12, 14) to cancel.

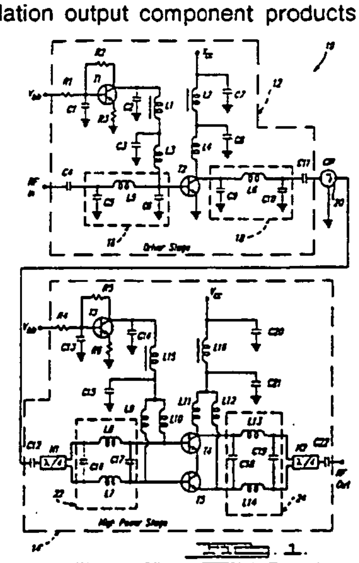

FIG. 1.

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SELF EQUALIZING MULTI-STAGE RADIO FREQUENCY POWER AMPLIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to radio frequency power amplifiers and, more particularly, to a method to be used within a radio frequency multi-stage power amplifier to increase linearity and efficiency of the amplifier.

2. Discussion

Multi-stage radio frequency power amplifiers are used in a wide variety of communications and other electronic applications. These amplifiers are made up of two or more cascaded amplifier stages, each of which increases the level of the signal applied to the input of that stage by an amount known as the stage gain. The multi-stage amplifier output is therefore a replica of the input signal increased by the product of the stage gains. Ideally the input to output transfer of each stage would be linear; a perfect replica of the input signal, increased in amplitude, would appear at the amplifier output. Practical amplifiers, however, have a degree of non-linearity in their transfer characteristic. This non-linearity results in the distortion of the output signal so that it is no longer a perfect amplified replica of the input. One manifestation of this distortion is the creation of spurious signal components, known as intermodulation products, at frequencies which did not exist at the original input. These intermodulation components have a deleterious effect on the performance of the system employing the power amplifiers.

Two principal approaches have previously been used to increase linearity and thereby reduce the generation of intermodulation products. The first is the class A operation of each of the amplifier stages. This class of operation features the highest linearity but is often impractical because of its very poor efficiency and high thermal dissipation characteristics. The second conventional approach is the employment of separate linearizer circuits. Feed-forward, feed-back, and pre-distortion linearizers are conventionally utilized for this application. The separate linearizer approach suffers from several significant disadvantages. It significantly increases the cost of the amplifier and requires complex tuning and alignment to track the inherent variations of the amplifier over time and environmental changes. Additionally, the degree of linearization possible with a multi-stage amplifier is limited by the non-linear combination of the distortions generated by each stage.

The present invention overcomes the inherent disadvantages of the conventional approaches. The amplifier is designed so that the intermodulation components generated in each pair of cascaded stages are of opposite phase. In this manner the intermodulation components will combine subtractively thereby reducing the component level over the range of operation of the amplifier.

SUMMARY OF THE INVENTION

According to the teachings of the present invention, linearity and distortion of the radio frequency multi-stage power amplifier is improved by employing circuit means for internally causing the intermodulation output components associated with the individual stages to be 180° out of phase thereby resulting in cancellation.

The method to be utilized in eliminating the intermodulation output components associated with this multi-stage radio frequency power amplifier employs generally two steps. In the first step, the high power output stage is optimized for efficiency, linearity, and power output. This optimization procedure incorporates the following steps: (1) selection of the amplifier device (transistor); (2) selection of the amplifier device bias voltages; (3) design of the input and output tuned matching circuits; and (4) design of the bias circuits. After this optimization is completed, step two employs the appropriate selection of values of elements defining the input and output tuned circuits associated with the driver stage of the multi-stage radio frequency power amplifier. By appropriate element selection of these tuned circuits, the inter-

modulation output components associated with the driver stage will be out of phase with the high power stage intermodulation components.

BRIEF DESCRIPTION OF THE DRAWINGS

The various advantages of the present invention will become apparent to those skilled in the art by reading the following specification and by reference to the drawings in which:

FIG. 1 is an electronic schematic circuit diagram of a two stage radio frequency power amplification device made in accordance with the teachings of the preferred embodiment of this invention;

FIG. 2 is a graphical illustration helpful in understanding the tuning of the output stage in accordance with the teachings of the preferred embodiment of the invention;

FIG. 3 is a graphical illustration of the output power level and associated intermodulation power level and phase angle of the driver stage after tuning in accordance with the teachings of this invention; and

FIG. 4 is a graphical illustration of the power level and phase angle associated with the intermodulation components of the output and driver stages of the amplifier for a given output power signal after the method of this invention has been performed.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning now to FIG. 1, a two stage amplifier 10 having a driver stage 12 and a high power output stage 14 is illustrated. Radio frequency signals are input into amplifier 10 through capacitor C_4. The purpose of C_4 is to act as a direct current block. Further traversing the device, the signal then goes through the first input tuned circuit 16 associated with the driver stage 12. This input tuned circuit 16 consists of inductor L_5, and capacitors C_5 and C_6. Transistor T_2 amplifies the input signal and passes it to the input of the output tuned circuit 18.

Direct current voltage V_{bb} is impressed on resistor R_1. The combination of resistors R_1, R_2, and R_3 along with capacitor C_1 acts to bias transistor T_1. Voltage appears at the collector of T_1 and is transferred to the base of transistor T_2 for biasing purposes. This transfer of collector voltage from transistor T_1 is effectuated by means of inductors and L_1 and L_3. Capacitors C_2, C_3, act as alternating current shunts to ground. The collector of transistor T_2 is biased by direct current voltage V_{cc} via inductors L_2 and L_4. Capacitors C_7 and C_8 act as alternating current shunts to ground.

The output tuned circuit 18 associated with the driver stage 12 is defined by inductor L_5, and capacitors C_9 and C_{10}. Capacitor C_{11} acts as a direct current block and connects the output of the driver stage to the circulator device 20. The circulator provides radio frequency isolation between the driver stage 12 and the high power stage 14 of the radio frequency power amplifier 10.

The output of the circulator device is connected to capacitor C_{12} which acts as a direct current block. The output of capacitor C_{12} goes into a hybrid circuit designated as H_1. This hybrid circuit takes the single ended output of capacitor C_{12} and converts this output to a balanced signal. The output of hybrid circuit H_1 serves as the dual input to the input tuned circuit of the high power output stage 14. The input tuned circuit 22 associated with the high power stage 14 is made up of inductors L_7 and L_8 and capacitors C_{16} and C_{17}. The amplification device associated with the high power stage is a push-pull dual transistor arrangement of T_4 and T_5.

Transistor T_3 is biased by means of resistors R_4, R_5, and R_6, direct current voltage V_{bb}, and capacitor C_{13}. The output voltage associated with the collector of transistor T_3 is transferred to the base of transistors T_4 and T_5 for biasing purposes. The voltage associated with the collector of transistor T_3 is transferred to the base of transistor T_4 by means of inductors L_{10} and L_{15}. Capacitors C_{14} and C_{15} shunt any undesired alternating current to ground. The transfer of voltage from the collector of transistor T_3 to the base of transistor T_5 is accomplished by inductors L_9 and L_{15}. Direct current voltage V_{cc} is transferred to the collectors of transistors T_4 and T_5 for biasing purposes. This transfer of voltage to the collector of transistor T_4 is accomplished by inductors L_{16} and L_{11}. Capacitors C_{20} and C_{21} shunt any undesired alternating current to ground. The transfer of voltage from voltage source V_{cc} to the collector of transistor T_5 is accomplished by means of inductors L_{12} and L_{16}.

The output tuned circuit 24 associated with this high power stage 14 includes inductors L_{13} and L_{14} and capacitors C_{18} and C_{19}. The output signal of this output tuned circuit 24 is then connected to a hybrid

circuit H_2. Hybrid circuit H_2 converts the signal from a balanced type signal to a single ended signal. The output of hybrid H_2 is then connected to capacitor C_{22} for direct current blocking purposes. The output of capacitor C_{22} is the radio frequency power output signal associated with the two stage radio frequency power amplification device 10.

The method of the present invention can best be understood by way of a simplified example. With reference to FIG. 1, one would select element values for inductors L_7, L_8, L_{14}, and L_{13} along with element values for capacitors C_{16}, C_{17}, C_{18}, and C_{19} in order to maximize the power output, efficiency, and linearity of the high power stage 14 of this radio frequency power amplifier. In practice this is accomplished by applying an input test signal made up of two equal amplitude sine waves whose frequencies are slightly offset to the high power output stage 14. As the power level of the input is increased, the level of the output signal and intermodulation components are measured. The results of a typical measurement are shown in FIG. 2 as curve set 1. As an example, the required output power, which is specified by the application, is also indicated in the figure. Other tuning and bias conditions will provide the same output power for different levels of input power, direct current to radio frequency conversion efficiencies, and carrier to intermodulation power ratios as indicated in the figure as curve sets 2 and 3. For each selection of element values for the input and output tuned circuits 22, 24 of the high power stage 14, the intermodulation power as a function of input power relationship shows a null as input power is increased. The phase of the intermodulation products for input levels below the null is opposite to the phase above the null as portrayed by the "+" and "-" symbols in FIG. 2. As the high power stage is optimized for higher output power, the null shifts to the right and the intermodulation characteristic behaves as shown in FIG. 2. The tuning of the high power stage is based on selecting the best compromise between the direct current to radio frequency conversion efficiency and the carrier to intermodulation power ratio. This tuning results in placing the null to the right of the point where the output signal reaches the required output power level. Using this criterion, the tuning corresponding to curve 2 would be selected, since the intermodulation null is to the right of this point where the output signal reaches the required output power level.

Once these elements have been selected and the efficiency, linearity, and power output of the stage 14 has been optimized one would then select element values for the input and output tuned circuits 16, 18 of the driver stage 12. These circuits are comprised of inductors L_5 and L_6 and capacitors C_5, C_6, C_9, and C_{10}. The values of these elements are chosen to cause the intermodulation distortion output components associated with the driver stage 12 to be at a 180° phase angle from the intermodulation distortion output components associated with the high power stage 14. These intermodulation output components of the driver stage 12 will cancel the intermodulation output components in the high power stage 14. This cancellation of intermodulation output components will result in the overall radio frequency power amplification device 10 having a greater linearity and greater efficiency than before.

In practice this is accomplished by having the driver stage amplifier initially designed and characterized using the same procedure as the output stage. The family of signal input, output, and intermodulation characteristics for the various tunings and bias condition is determined. The tuning and bias condition selected for the driver state is that which produces the necessary output power with the intermodulation power null to the left of the desired operating point as shown in Fig. 3. Thus, the intermodulation products resulting from the driver stage are in phase opposition to those of the output stage over the operating region. Note the null to the left of the operating point. The resultant operational characteristics of the two stage amplifier is shown in FIG. 4. For power input levels between the two nulls the output intermodulation components of the two stage amplifier will be reduced or eliminated because the associated intermodulation output components of the driver (input) stage and the output stage are of opposite phase in this region of operation as indicated by the "+" and "-" symbols.

The following Table I sets forth representative values and descriptions of some of the elements of device 10 that have provided satisfactory results.

TABLE I

1.) Driver Stage	
Item	Description/Value
T_2	MRA 0204-60VH
C_5	2.6 p.f.
C_6	18 p.f.
L_5	16 n.h.
C_9	71 p.f.
C_{10}	7.5 p.f.
L_6	13.5 n.h.
2.) Output Stage	
T_4	MRT 0204-110V
T_5	MRT 0204-110V
C_{16}	18 p.f.
C_{17}	82 p.f.
L_7	7 n.h.
L_8	7 n.h.
C_{18}	150 p.f.
C_{19}	30 p.f.
L_{13}	13 n.h.
L_{14}	13 n.h.

In view of the foregoing, it can be appreciated that the present invention enables the user to achieve high linearity and high efficiency of his multi-stage radio frequency power amplifier device by selecting values for internal components associated with the device. Thus, while this invention has been described in connection with a particular example thereof, no limitation is intended thereby except as defined by the following claims. This is because the skilled practitioner will realize that other modifications can be made without departing from the spirit of this invention after studying the specification and drawings.

Claims

1. A radio frequency power amplifier circuit having a driver stage (12) coupled to a high power stage (14), each stage (12, 14) having intermodulation distortion output components, characterized by:
- circuit means for internally defining the intermodulation distortion components of the output of the driver stage (14) such that said components are 180° out of phase with the intermodulation distortion components of the output of the individual high power stage (14) whereby the intermodulation distortion component outputs of the two stages (12, 14) will subtract from or cancel each other.

2. The circuit of claim 1, characterized in that the circuit means comprises:
- two tuned circuits ($C_5/L_5/C_6$, $C_9/L_6/C_{10}$) connected to a transistor (T_2) in the driver stage (12), said tuned circuits ($C_5/L_5/C_6$, $C_9/L_6/C_{10}$) having elements with values chosen to cause intermodulation component outputs of said driver stage (12) to cancel with intermodulation component outputs of the high power stage (14), and
- two tuned circuits ($C_{16}/L_7/L_8/C_{17}$, $C_{18}/L_{13}/L_{14}/C_{19}$) connected to at least one transistor (T_4, T_5) in the high power stage (14), said tuned circuits ($C_{16}/L_7/L_8/C_{17}$, $C_{18}/L_{13}/L_{14}/C_{19}$) having elements with values chosen to optimize the high power stage (14) for efficiency, linearity, and power output.

3. The circuit of claim 1 or 2, characterized in that said circuit means comprises bipolar transistors (T_1-T_5).

4. The circuit of claim 1 or 2, characterized in that said circuit means comprises FET-transistors.

5. The circuit of any of claims 2 through 4, characterized in that said tuned circuits ($C_5/L_5/C_6$, $C_9/L_6/C_{10}$; $C_{16}/L_7/L_8/C_{17}$, $C_{18}/L_{13}/L_{14}/C_{19}$) each comprises an inductive capacitive network.

6. The circuit of any of claims 1 through 5, characterized in that said high power stage (14) comprises a push-pull amplifier (T_4, T_5).

7. The circuit of any of claims 1 through 6, characterized in that said driver stage (12) and said high power stage (14) of said radio frequency amplifier (10) are connected together by means of a circulator device (20).

8. The circuit of any of claims 1 through 7, characterized by hybrid circuit means (H_2) connected to the output of said high power stage (14) to convert an output signal of said high power stage (14) from balanced to single ended and, hybrid circuit means (H_1) connected to the input of said high power stage (14) to balance the input signal.

9. A power amplification circuit, characterized by:

a) a driver stage (12) including:

- an input tuned circuit (16) connected to the input of a transistor (T_2); an output tuned circuit (18) connected to the output of said transistor (T_2);
- biasing means ($R_1/C_1/R_2/T_1/C_2/L_1/C_3/L_3/L_2/C_7/L_4/C_8$) connected to the transistor (T_2) for biasing the transistor (T_2); and
- capacitive circuit means (C_4, C_{11}) connected to the input and to the output of the driver stage (12) to block direct current;

b) a high power stage (14) including:

- capacitive circuit means (C'_2, C_{22}) connected to the input and to the output of the high power stage (14) to block direct current;
- a dual transistor push-pull amplifier circuit (T_4/T_5);
- an output tuned circuit (24) connected to the output of the push-pull dual transistor amplifier (T_4/T_5);
- an input tuned circuit (22) connected to the input of the push-pull dual transistor amplifier (T_4/T_5);
- biasing means ($R_4/C_{13}/R_5/T_3/R_6/C_{14}/L_{15}/C_{15}/L_9/$ $L_{10}/C_{20}/L_{16}/C_{21}/L_{11}/L_{12}$) for biasing the transistors (T_4, T_5) in the dual transistor push-pull amplifier circuit (T_4/T_5); and
- first hybrid circuit means (H_1) connected to the input of the input tuned circuit (22) to balance the input signal and second hybrid circuit means (H_2) connected to the output of the output tuned circuit (24) to convert the output signal from balanced to single ended;

c) a circulator device (20) connecting the output of the driver stage (12) to the input of the high power stage (14) to provide electrical isolation; and

d) said tuned circuits (16, 18) in the driver stage (12) having elemental values chosen to cause the intermodulation distortion components of the output of the driver stage (12) to have a phase angle which is 180° opposite from the phase angle associated with the intermodulation distortion components of the output of the individual high power stage (14).

10. The circuit of claim 9, characterized in that the input and output tuned circuits (16, 18) of the driver stage (12) are comprised of inductive-capacitive networks ($C_5/L_5/C_6$, $C_9/L_6/C_{10}$).

11. The circuit of claim 9 or 10, characterized in that the input and output tuned circuits (22, 24) of the high power stage (14) comprise inductive-capacitive networks ($C_{16}/L_7/L_8/C_{17}$, $C_{18}/L_{13}/L_{14}/C_{19}$)

12. A method of combining stage (12, 14) of a multistage solid state radio frequency power amplifier (10) together in order to eliminate intermodulation components which are attributable to the outputs of each of the individual stages (12, 14), characterized by:

a) tuning a high power stage (14) for efficiency, linearity and power output; and

b) tuning a driver stage (12) such that the intermodulation components which are produced are of an alternate phase angle than the intermodulation components produced in the individual high power stage (14) such that the intermodulation output components of the stages (12, 14) will subtract from each other or cancel.

13. The method of claim 12, characterized in that said high power stage (14) includes at least one transistor (T_4, T_5) with an input and and output tuned circuit (22, 24) connected thereto.

14. The method of claim 13, characterized in that said step (a) includes selecting element values of said input and output tuned circuits (22, 24) in order to optimize the efficiency, linearity and power output of said high power stage (14).

15. The method of any of claims 12 through 14, characterized in that said driver stage (12) includes at least one transistor (T_2), with an input and output tuned circuit (16, 18) connected thereto.

16. The method of claim 15, characterized in that step (b) includes the selection of element values for said input tuned circuit (16) of the driver stage (12) and values for said output tuned circuit (18) of the driver stage (12) in order to cause the phase angles of the intermodulation distortion output components associated with said driver stage (12) to be at a 180° angle relative to the distortion output components of the individual high power stage (14).

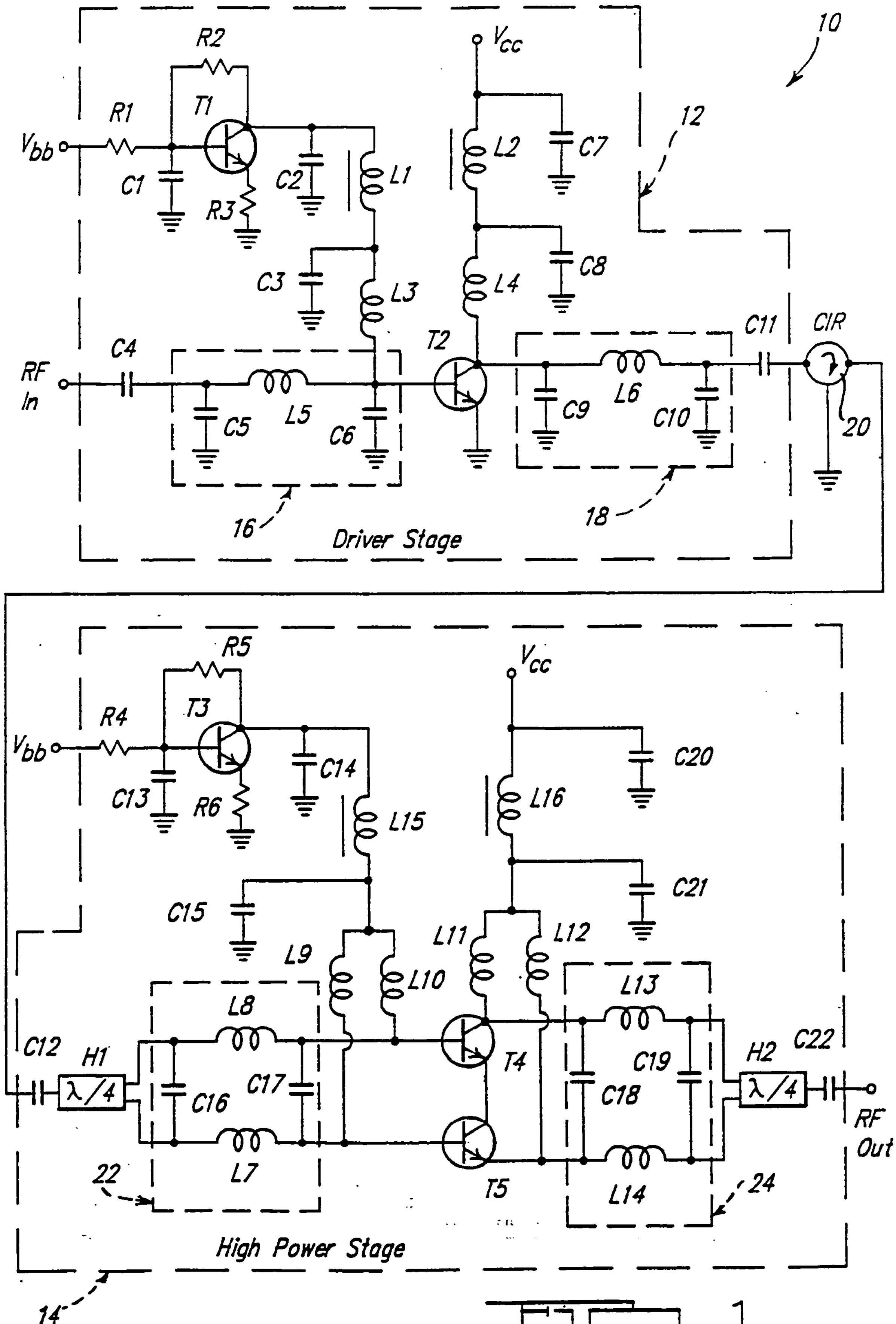

FIG. 1.

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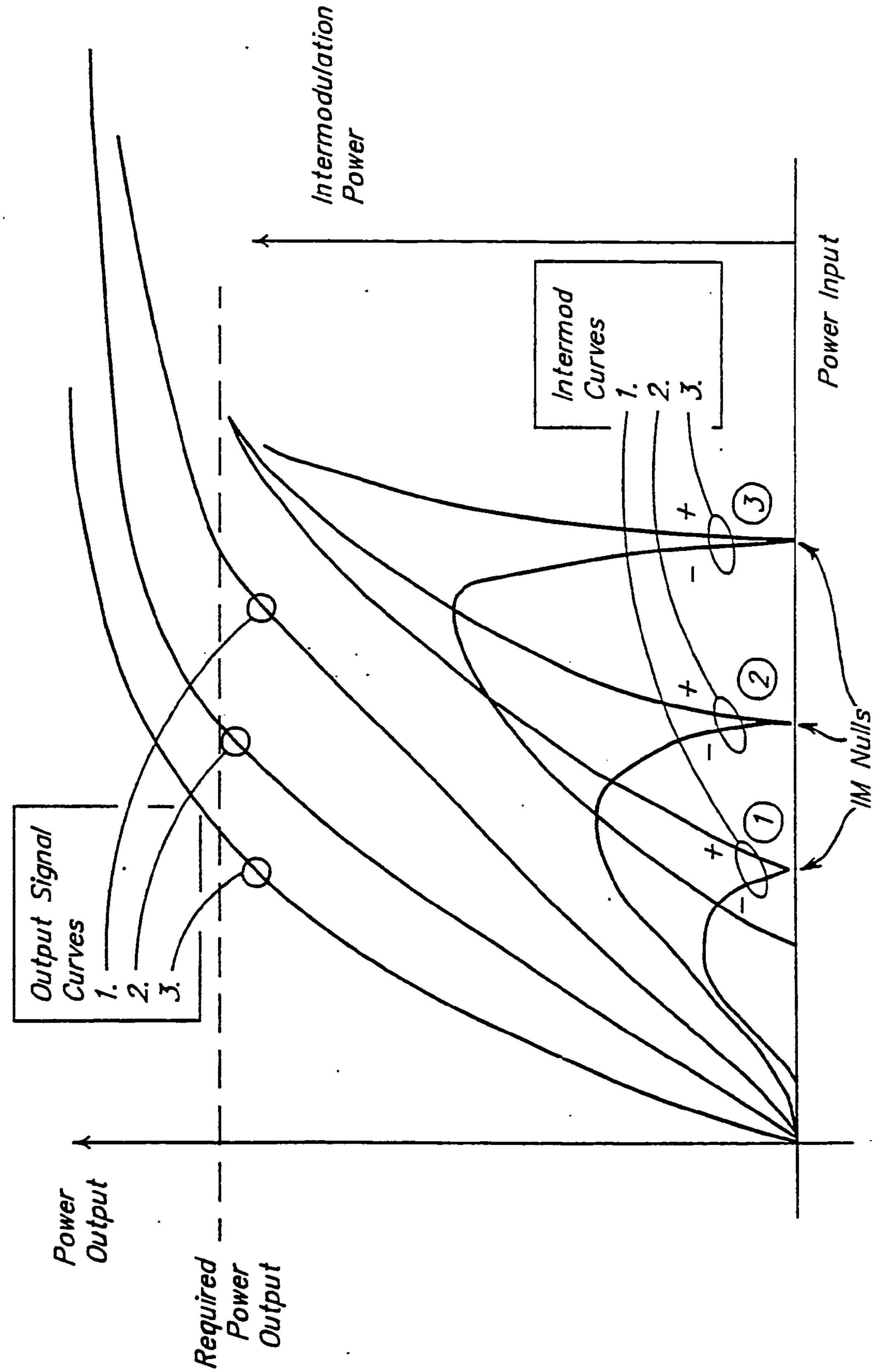

FIG. 2. OUTPUT STAGE CHARACTERISTICS

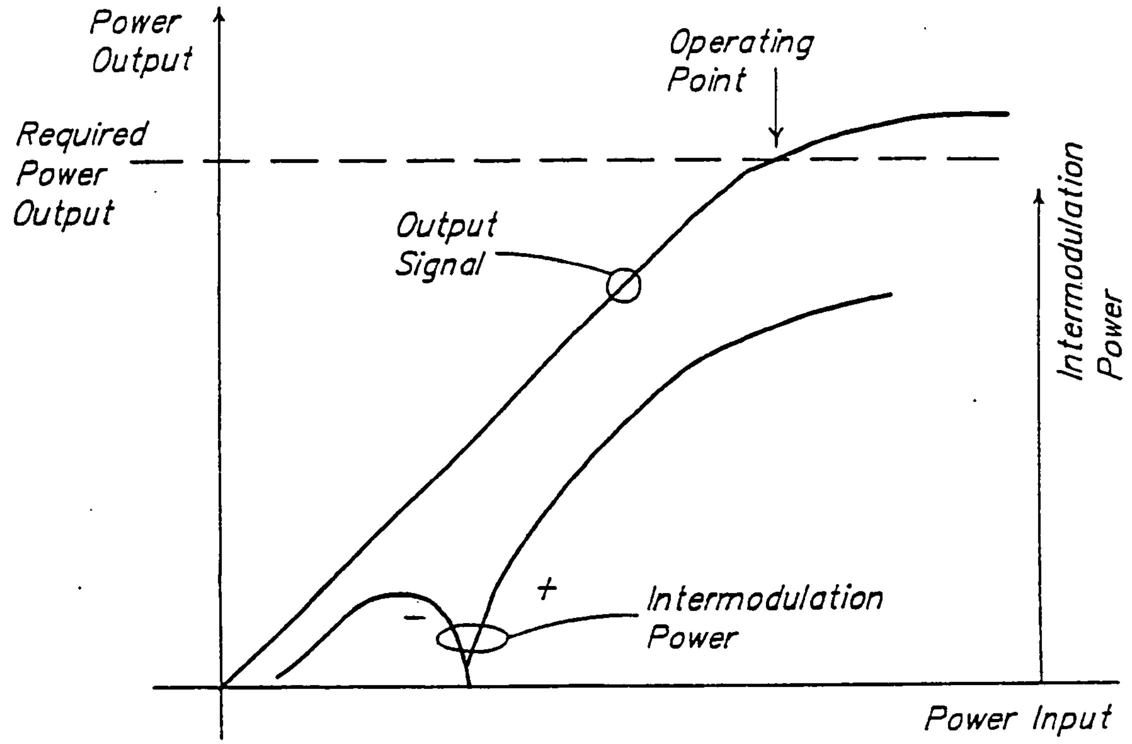

FIG. 3. DRIVER STAGE CHARACTERISTICS

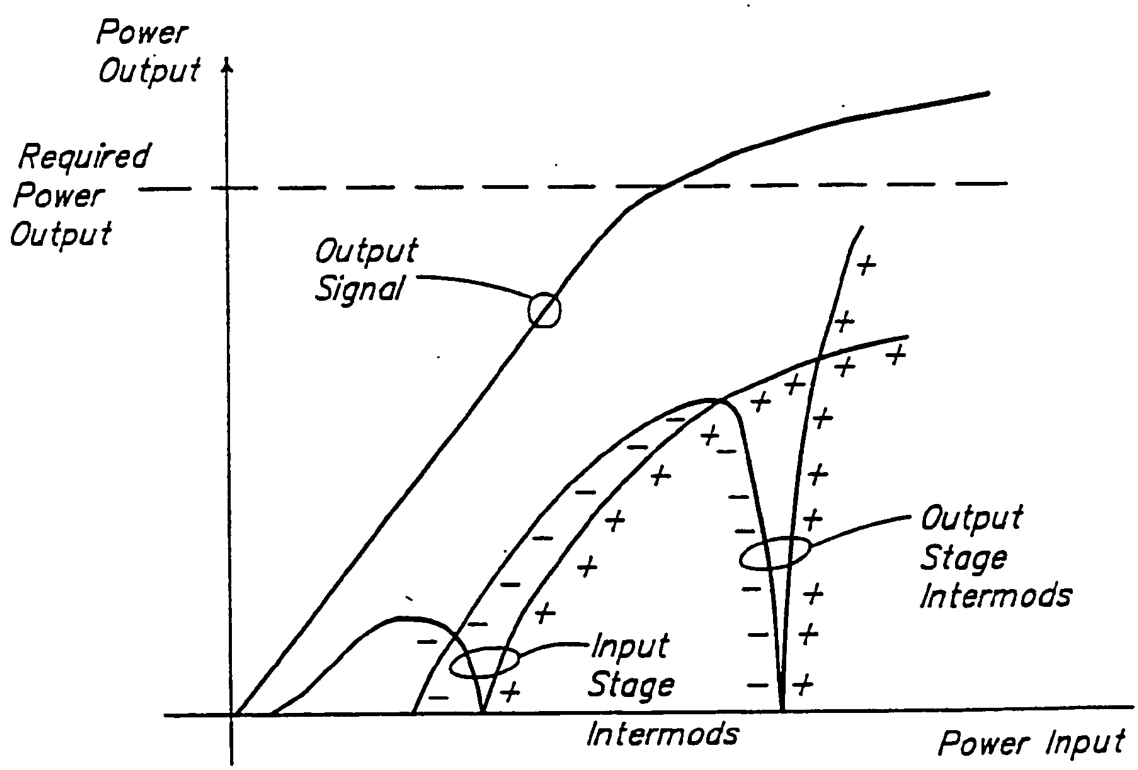

FIG. 4. TWO STAGE CHARACTERISTICS

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(71) Applicant: **Hughes Aircraft Company**
7200 Hughes Terrace P.O. Box 45066
Los Angeles, California 90045-0066(US)

(72) Inventor: **Berman, Arnold L.**
714 Claymont Drive
Los Angeles California 90049(US)
Inventor: **Hahn, Carl J., III**
430 West 64th Street
Inglewood California 90302(US)
Inventor: **Wachs, Marvin R.**
22555 Paul Revere Drive
Woodland Hills California 91364(US)

(74) Representative: **Witte, Alexander, Dr.-Ing.**
Augustenstrasse 7
W-7000 Stuttgart 1(DE)

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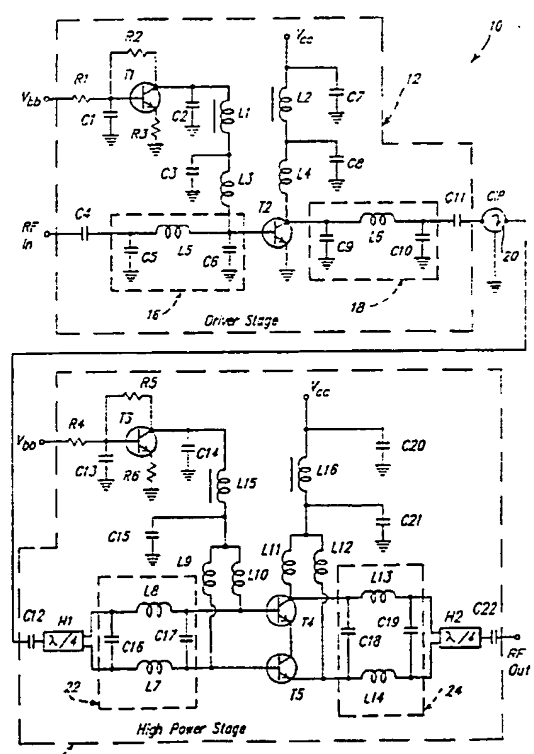

FIG. 1.

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EUROPEAN SEARCH REPORT

Application Number

EP 89 12 0854

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 243 898 (ROHDE & SCHWARZ GmbH & CO. KG) * Figure 1; page 1, line 9 - page 2, line 22 *	1,3,4	H 03 F 1/32
A	DE-A-1 955 727 (RICHARD HIRSCHMANN RADIOTECHNISCHES WERK) * Figures 4,7; page 7, line 9 - page 8, line 21; page 9, line 2 - page 11, line 15 *	2,3,5, 9-12	
A	EP-A-0 289 130 (RACAL COMMUNICATIONS EQUIPMENT UNITED) * Column 2, line 34 - column 3, line 7; cclumn 4, lines 38-50 *	1,6	
A	DE-A-3 133 673 (SIEMENS AG) * Page 2, lines 13-18 *	1,3	
A	IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE, Atlanta, Georgia, 26th - 29th November 1984, vol. 3, pages 1246-1252; H. IGARASHI et al.: "GaAs fet power amplifier for 6 GHz SSB radio" * Figure 1 *	7,8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 03 F

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	17 December 90	WALDORFF U.

CATEGORY OF CITED DOCUMENTS

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